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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/820,691	04/08/2004	Robert A. Abraham	10031136-1	8538

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AGILENT TECHNOLOGIES, INC.
Legal Department, DL429
Intellectual Property Administration
P.O. Box 7599
Loveland, CO 80537-0599

EXAMINER

GOODLEY, JAMES E

ART UNIT	PAPER NUMBER
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2817

DATE MAILED: 08/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/820,691

Applicant(s)

ABRAHAM ET AL.

Examiner

James E. Goodley

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 08 April 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☒ Claim(s) 8 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 4/8/2004.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Claim Objections

Claim 8 is objected to because of the following informalities: there is no antecedent basis for "the voltage shift-down mechanism". It appears that claim 8 should depend from claim 4 instead of claim 2. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-5 and 15-20 are rejected under 35 U.S.C. 102(b) as being anticipated by *Lo et al. (US 6,046,646)*, hereinafter Lo.

Regarding **claims 1-5, and 15-18**, lines 8-15 of column 3, lines 1-11 of column 6, and Fig. 6 of Lo show a method for reducing EMI in a spread spectrum clock generation PLL circuit comprising: a voltage controlled oscillator (VCO) [324] that includes an input [317] coupled to a voltage control node [input to VCO] and an output [326] for generating a spread spectrum clock signal $[F_{VCO}]$ with a frequency which is proportional to the input control voltage and a VCO input voltage modulation mechanism [330'] coupled to the input voltage control node for modulating the voltage at the control node by including in the voltage modulation mechanism: a voltage shift-up mechanism [334']

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for pulling up the voltage at the VCO input node by injecting current into that node, wherein the modulation mechanism generates a shift-up control signal [triangular input directly to left of switch to engage 334'] to input to the shift-up mechanism and a shift-up control enable signal [346] to input to the shift-up mechanism; and similarly, a voltage shift-down mechanism [336'] for pulling down the voltage at the VCO input node by drawing current from that node, wherein the modulation mechanism generates a shift-down control signal [triangular input directly to left of switch to engage 336'] to input to the shift-down mechanism and a shift-down control enable signal [348] to input to the shift-down mechanism.

Regarding **claims 19-20**, Fig. 6 of Lo shows the method of claim 1 further comprising a P-counter [328] that includes an input coupled to the VCO [324], a register for storing a single P value [flip-flop 328] and an output [310]; a Q-counter [304] that includes an input [302] for receiving a reference frequency [F_{ref}] and an output [306]; a phase detector [308] that includes a first input [306] coupled to the output of the Q counter and a second input [310] coupled to the output of the P counter and an output ["UP"] for generating a control signal [317]; a charge pump [312] coupled to the phase detector for receiving the control signal and selectively charging and discharging the voltage control node based on the control signal; and a loop filter [318].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

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(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 6-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lo in view of *Tiede (US 6,736,474)*.

Regarding **claims 6-7**, Lo shows the circuit of claim 2 showing a voltage shift-up current source except, "wherein the voltage shift-up mechanism includes a first transistor having a drain electrode coupled to a first predetermined voltage, a source electrode, and a gate electrode for receiving a first shift-up control signal; a second transistor having a drain electrode coupled to the source electrode of the first transistor, a source electrode coupled to the VCO input voltage node, and a gate electrode for receiving a shift-up control enable signal; a plurality of transistors coupled in parallel to the first transistor; wherein each transistor includes a drain electrode that is coupled to the first predetermined voltage, a source electrode that is coupled to the drain electrode of the second transistor, and a gate electrode for receiving a corresponding shift-up control signal". However, lines 36-53 of column 2 and Fig. 3 of Tiede show a voltage shift-up mechanism [70] including a first transistor [90] having a drain electrode coupled to a first predetermined voltage V_{PWR} , a source electrode and a gate electrode for receiving a first shift-up control signal [80]; a second transistor [88] having a drain electrode coupled to the source electrode of the first transistor, a source electrode coupled to the VCO input voltage node [92], and a gate electrode for receiving a shift-up control enable signal [74]; a plurality of transistors [82 and 86] coupled in parallel to the first transistor wherein each transistor includes a drain electrode that is coupled to the

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first predetermined voltage, a source electrode that is coupled to the drain electrode of the second transistor, and a gate electrode for receiving a corresponding shift-up control signal.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the voltage shift-up mechanism in the circuit of Lo by including the particular current-sourcing arrangement of Tiede for the purpose of raising the voltage at the input of the VCO in the oscillator loop, thereby raising the oscillation frequency.

Regarding **claims 8-9**, Lo shows the circuit of claim 4, showing a voltage shift-down current source except, "wherein the voltage shift-down mechanism includes a first transistor having a drain electrode coupled to the VCO input voltage node, a source electrode, and a gate electrode for receiving a shift-down control enable signal; a second transistor having a drain electrode coupled to the source electrode of the first transistor, a source electrode coupled to a second predetermined voltage, and a gate electrode for receiving a shift-down control signal; a plurality of transistors coupled in parallel to the second transistor; wherein each transistor includes a drain electrode that is coupled to the source of the first transistor, a source electrode that is coupled to the second predetermined voltage, and a gate electrode for receiving a corresponding shift-down control signal". However, lines 59-67 of column 2 and Fig. 5 of Tiede show a voltage shift-down mechanism [100] including a first transistor [90] having a drain electrode coupled to the VCO input voltage node [92], a source electrode and a gate electrode for receiving a shift-down control enable signal [78]; a second transistor [88]

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having a drain electrode coupled to the source electrode of the first transistor, a source electrode coupled to a second predetermined voltage [V_{gnd}], and a gate electrode for receiving a shift-down control signal [84]; a plurality of transistors [82 and 86] coupled in parallel to the first transistor wherein each transistor includes a drain electrode that is coupled to the source of the first transistor, a source electrode that is coupled to the second predetermined voltage, and a gate electrode for receiving a corresponding shift-down control signal.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the voltage shift-down mechanism in the circuit of Lo by including the particular current-sourcing arrangement of Tiede for the purpose of lowering the voltage at the input of the VCO in the oscillator loop, thereby lowering the oscillation frequency.

Claims 10-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lo in view of **Chang (US 6,606,005)**.

Regarding **claim 10**, Lo shows the circuit of claim 1 except being, "integrated in one of personal computers (PCs), computing devices, computer peripherals, office equipment, printers, network equipment, and other electronic applications where EMI reduction is needed". However, lines 13-23 in column 1 of Chang teach spreading the spectrum of a clock generator on the motherboard of a computer in order to reduce EMI.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a spread spectrum clock generator on a computer motherboard in order to reduce noise generated by a traditional clock.

Regarding **claims 11-12 and 14**, Lo shows the circuit of claim 1, except, "wherein the phase locked loop (PLL) modulation control circuit includes a plurality of programmable delay cells (PDCs) for generating the shift-up control signals and the shift-down control signals; wherein the time delay (Δt) of the delay cells is based on the modulation frequency and the number of modulation bits; wherein the delay cells are implemented as one of software and hardware." However, lines 23-28 of column 1, lines 50-59 of column 5 and Fig. 5A of Chang show a PLL programmable modulation circuit including a plurality of delay cells [35] for generating the shift-up [Vc1] and shift-down control [Vc2] signals; wherein the time delay of the delay cells is based on the modulation frequency and the number of modulation bits [2N].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the circuit of Lo by the circuit of Chang to implement a programmable array of hardware delay cells in a PLL circuit for generating shift-up and shift-down control signals for the purpose of more easily controlling current to the VCO.

Regarding **claim 13**, Lo in view of Chang discloses the circuit of claim 12, but does not specifically disclose "wherein the time delay of the delay cells are also determined by stability considerations for the PLL and the VCO characterization." However, it is inherent that the time delay constants of any components put into a

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phase locked feedback loop will always need to be subject to stability considerations in the loop as a whole in order for the loop to function as an oscillator.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Non-Patent literature document "**Charge-Pump Phase-Lock Loops**" by Floyd M. Gardner – IEEE Transactions on Communication, Vol. Com-28, No.11 November 1980.

Fax/Telephone Information

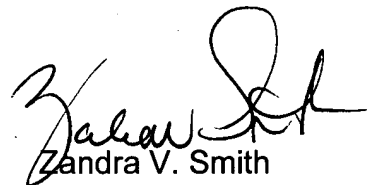
Any inquiry concerning this communication or earlier communications from the examiner should be directed to James E. Goodley. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert J. Pascal can be reached on (571)272-1769. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JG


Zandra V. Smith
Primary Examiner